IES/GATE

Electronics & Telecommunication Engineering

VOLUME-VIII

Advance Electronics, Microprocessor

Contents

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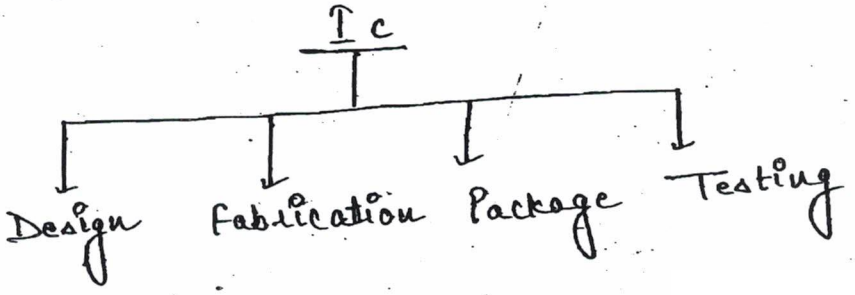

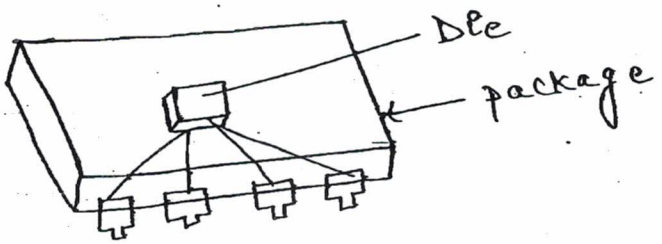

Syllaybus :-

(i) VLSI Tech :- Process, Lithography, Interconnects, Testing.

(ii) VLSI Design :- MUX/PROM/PLA circuit Design, Moore & Meelay Design; pipelining, DFT (Design for Testability)

(iii) Microprocessor: Basics, Instruction set, Instruction set, Interupts, DMA

(iv) Micro-controller :- (v) Embedded system :-

MUX/PROM/PLA :— ① Digital Design by John F. Wakerly
② Digital systems by Tocci
③ Digital Design (or) logic & computer design by Morris Mano

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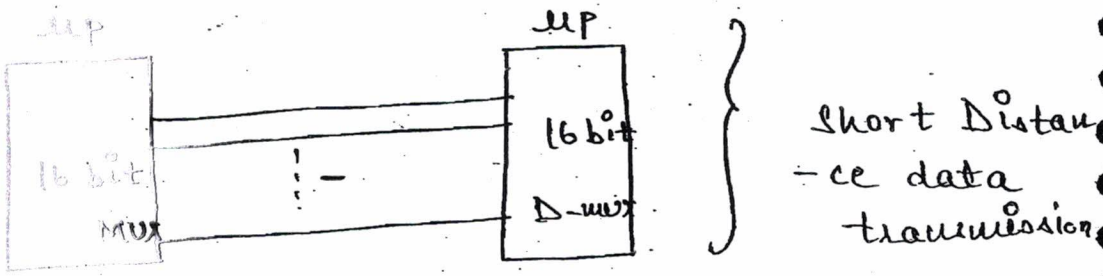
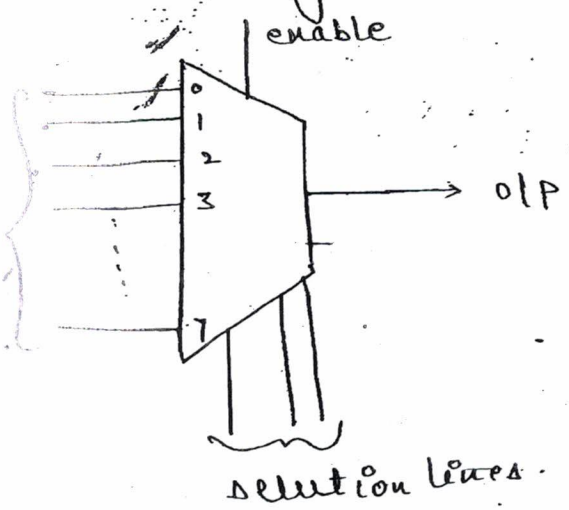
VLSI Design

(i) **MUX** :- Multiplexer is also called as data selector.



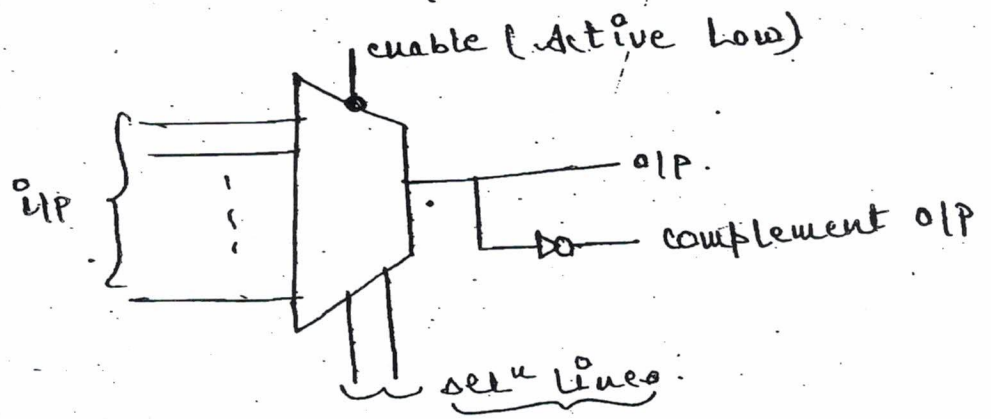
→ MUX is a combinational circuit.
→ It is having more than one input.
→ only one output.
→ having more than one selection lines.
→ This mux symbol.



In MUX

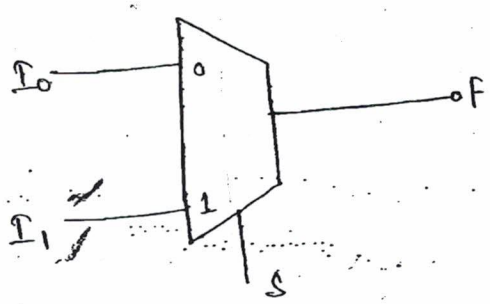
→ 2^n inputs.
→ n selection lines.
→ only one output.

⇒ Some of the mux o/p providing complementary outputs or low outputs.



⇒ mux also provide with enable pin.

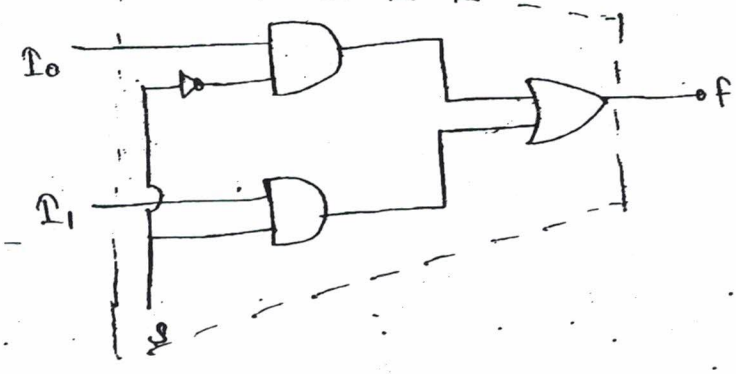
2X1 MUX



S	F
0	I_0
1	I_1

AND gate

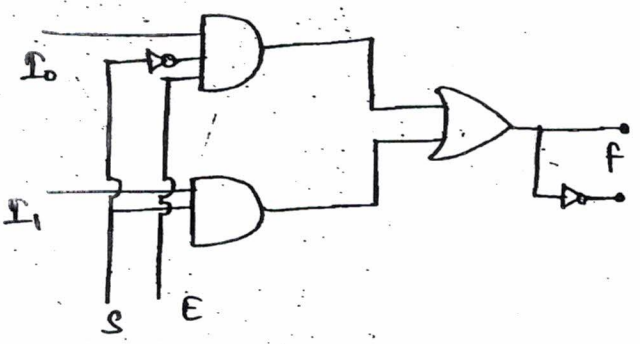
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



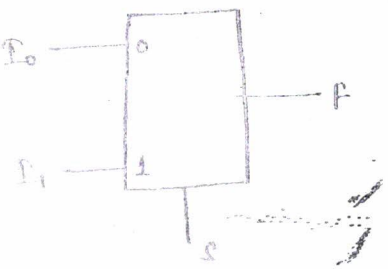
2:1 MUX

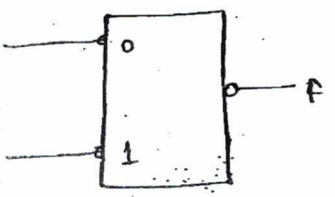
OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

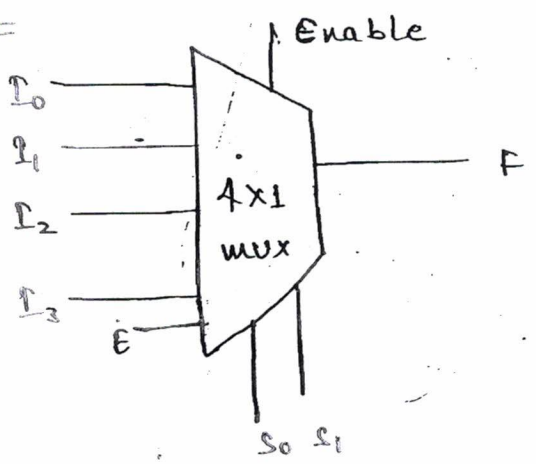


S	E	f
X	0	0
0	1	I0
1	1	I1



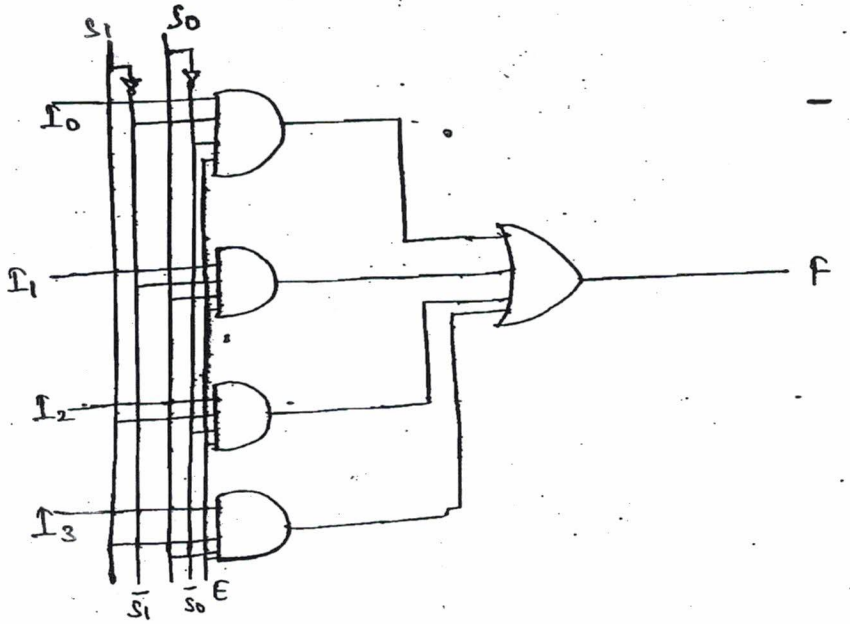


4x1 MUX

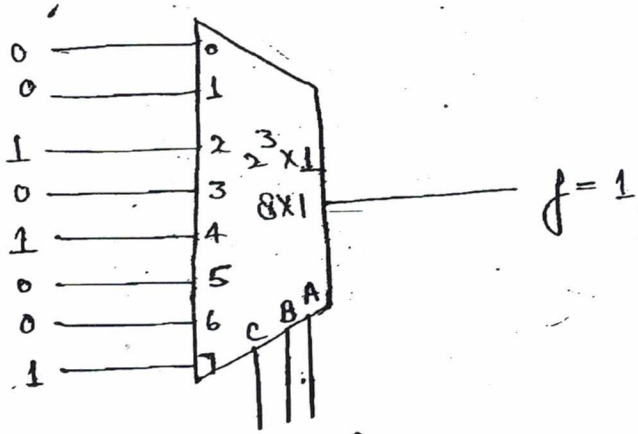


S_0	S_1	F
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

S_0	S_1	E	F
X	X	0	0
0	0	1	I_0
0	1	1	I_1
1	0	1	I_2
1	1	1	I_3



Ques: $f(A,B,C) = \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$ (010, 100, 111) implement using MUX.

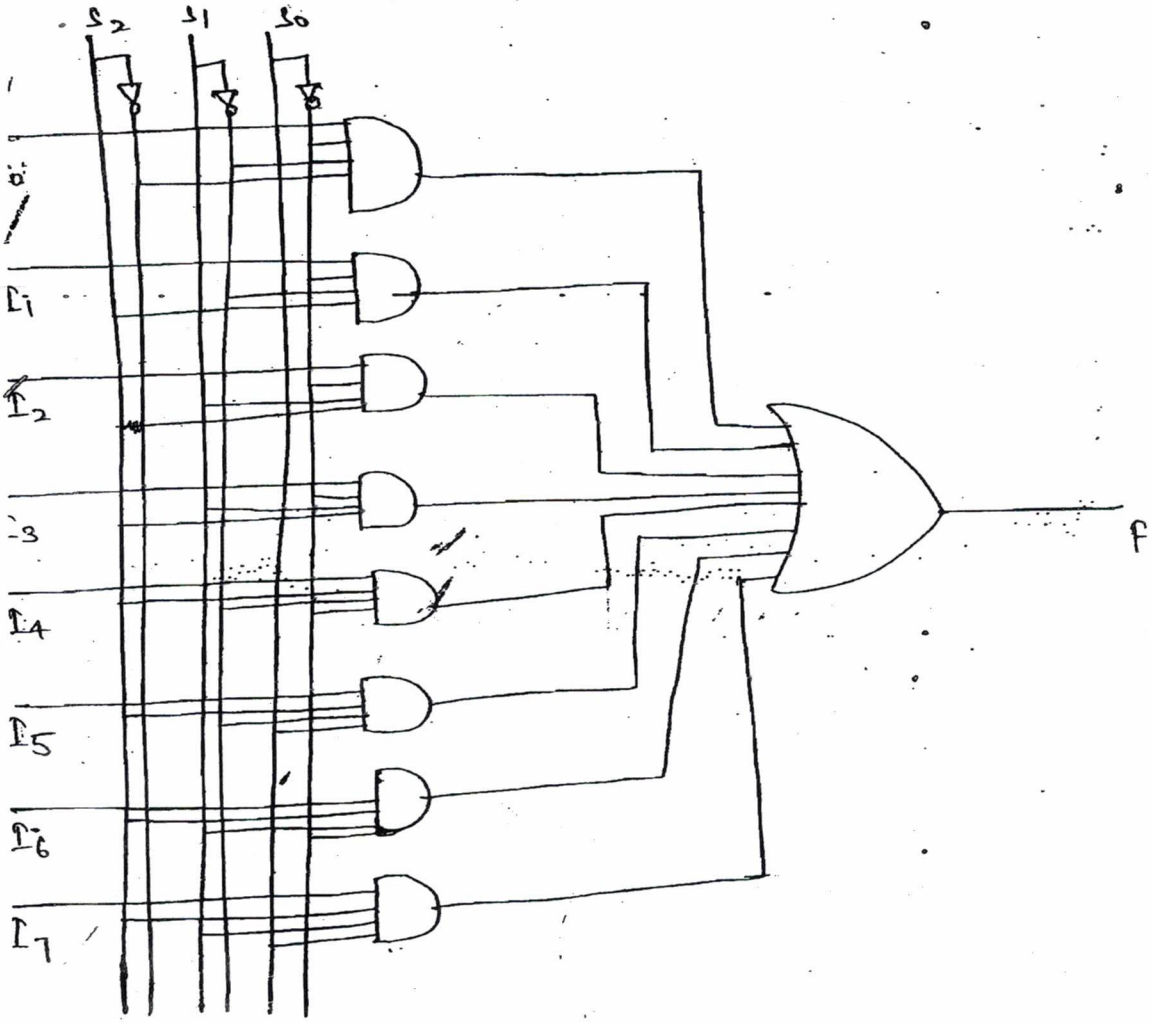


C	B	A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

* for implementing n variable function ⇒ min mux size needed is $2^{n-1} \times 1$

Ques: 1 $f(A,B,C) = \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$ using 4X1 mux.

8 X 1 mux using gates



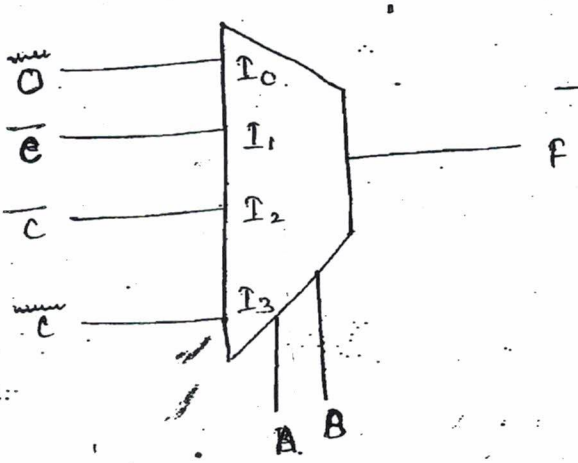
4x1 mux

A	B	C	Y
0	0	0 $\bar{C}$	0
0	0	1 C	0
0	1	0 $\bar{C}$	1
0	1	1 C	0
1	0	0 $\bar{C}$	1
1	0	1 C	0
1	1	0 $\bar{C}$	0
1	1	1 C	1

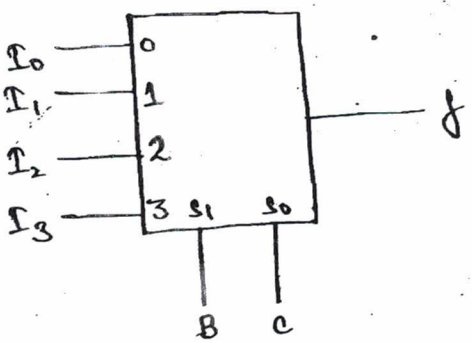
AB as select line

	I_0	I_1	I_2	I_3
$\bar{C}$	0	1	(2)	3
C	(4)	5	6	(7)
	$\bar{C}$	0	$\bar{C}$	$\bar{C}$

	I_0	I_1	I_2	I_3
$\bar{C}$	0	(2)	(4)	6
C	1	3	5	(7)
	0	$\bar{C}$	$\bar{C}$	C



Using BC as select line



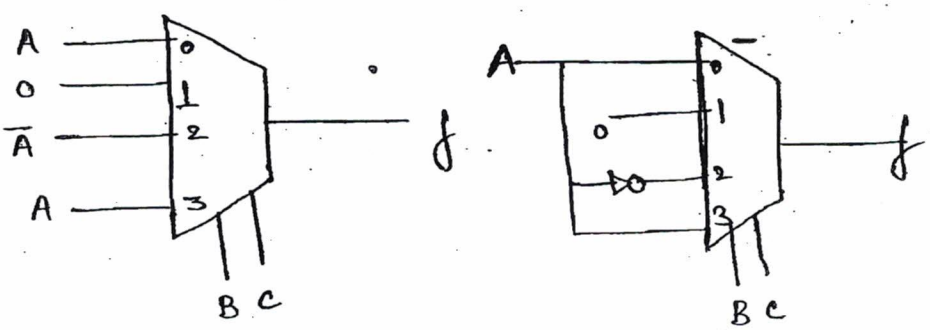
A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

SOP:- $f(A,B,C) = \Sigma(2,4,7)$ — (2)

POS:- $f(A,B,C) = \pi(0,1,3,5,6)$ — (1)

Implementation table

	I_0	I_1	I_2	I_3
$\bar{A}$	0	1	(2)	3
A	(4)	5	6	(7)
	A	0	$\bar{A}$	A

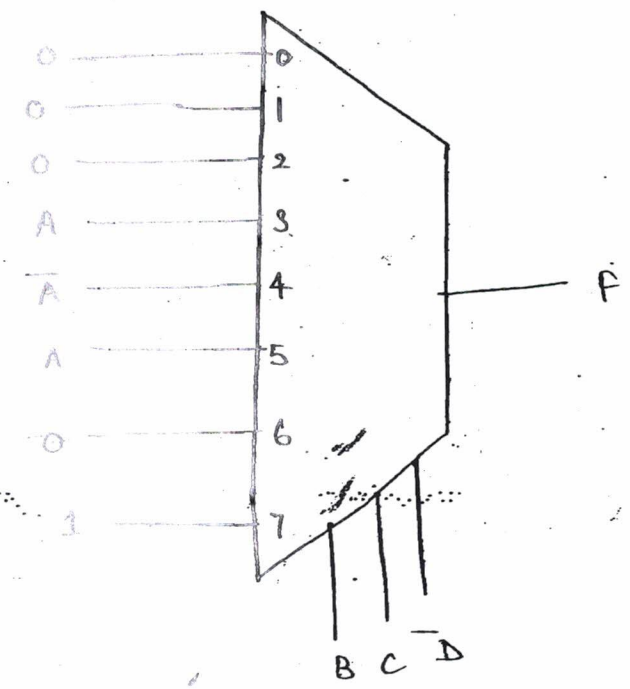


Qu: $f(A, B, C, D) = \Sigma(4, 7, 11, 13, 15)$ using 8×1.

A	B	C	D	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Implementation Table

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	1	2	3	(4)	5	6	(7)
A	B	9	10	(11)	12	(13)	14	(15)
	0	0	0	A	$\bar{A}$	A	0	1



sop :- $f(A,B,C) = \bar{A}B + \bar{A}B\bar{C} + \bar{B}C$

psop :- $f(A,B,C) = \bar{A}B\bar{C} + AB\bar{C} + ABC$ —

↓

Standard sum of product

from equ (1).

pos :- $f(A,B,C) = (A+B+C)(A+B+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+B+\bar{C}$

max terms

$(\bar{A}+\bar{B}$ RS 1/5

$f(A,B,C) = \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

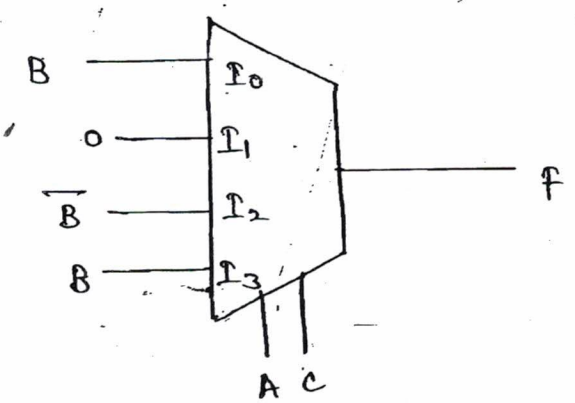
POS :- Max term funct^n

⇒ In mux it is not possible to implement POS funct^n. then find its equivalent min term funct^n SOP then implement it.

2:1 Ac as select line

Implementation table

	I_0	I_1	I_2	I_3
$\bar{B}$	0	1	④	5
B	②	3	6	⑦
	B	0	$\bar{B}$	B

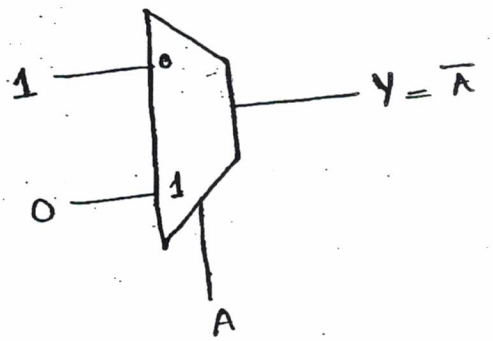


Qw: Implementation of logic gates using 2×1 mux.

① NOT gate

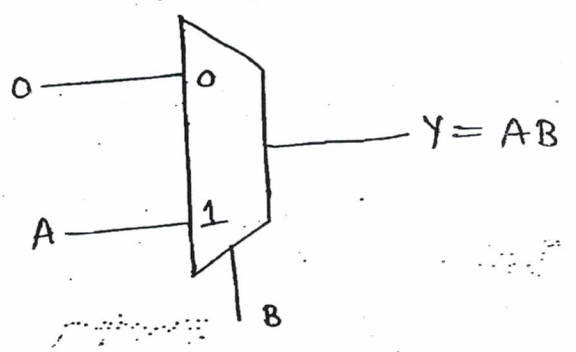
Truth Table

A	Y = $\overline{A}$
0	1
1	0



② AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

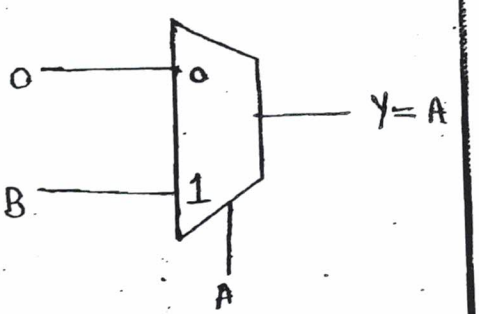


Implementation Table

	I_0	I_1
$\overline{A}$	0	1
A	2	③
	0	A

If A as select line

	I_0	I_1
$\overline{B}$	0	2
B	1	③
	0	R



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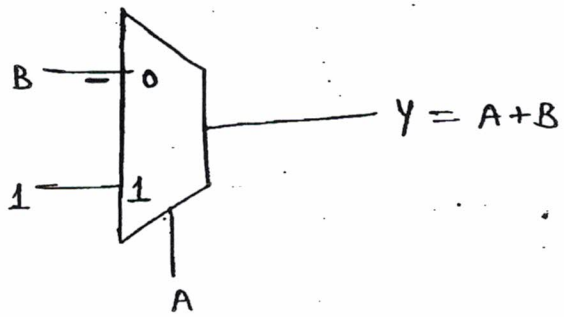
③ OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

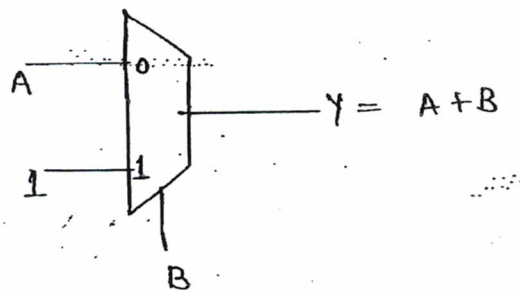
A as select line

	I_0	I_1
$\bar{B}$	0	②
B	①	③
	B	1



A B as select line

	I_0	I_1
$\bar{A}$	0	①
A	②	③
	A	1

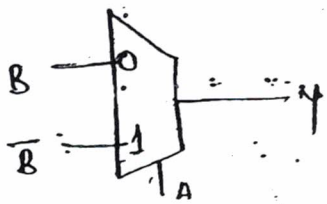


④ XOR = $\bar{A}B + A\bar{B} \Rightarrow A \oplus B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A as select line

	I_0	I_1
$\bar{B}$	0	②
B	①	3
	B	$\bar{B}$



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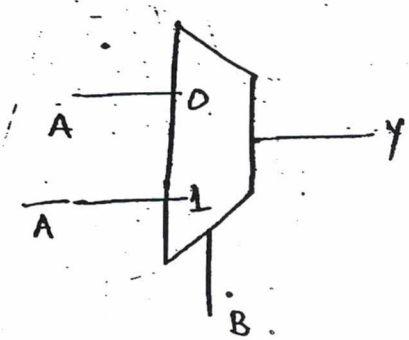
B as select line

	I_0	I_1
$\bar{A}$	0	(1)
A	(2)	3
	A	$\bar{A}$

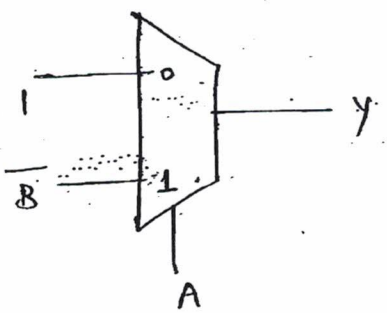


⑤ NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

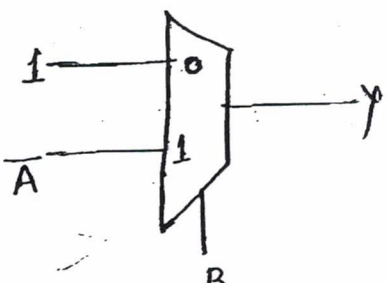
A as select line

	I_0	I_1
$\bar{B}$	(0)	(2)
B	(1)	3
	1	$\bar{B}$



B as select line

	I_0	I_1
$\bar{A}$	(0)	(1)
A	(2)	3
	1	$\bar{A}$

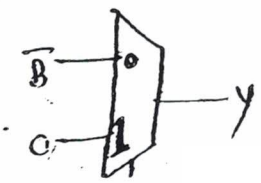


⑥ NOR gate

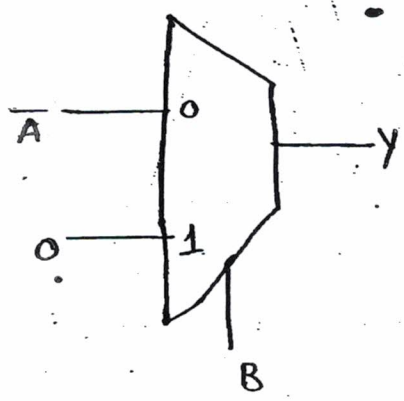
A	B	y
0	0	1
0	1	0
1	0	0

A as select line

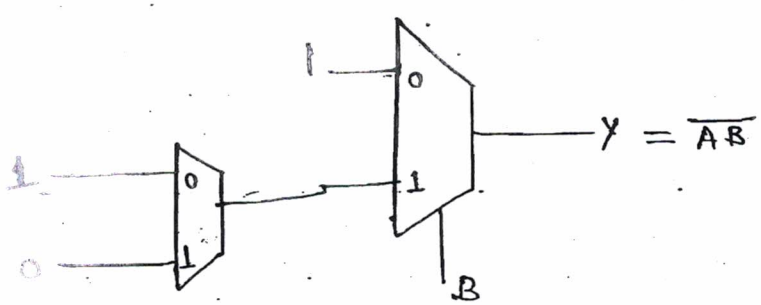
	I_0	I_1
$\bar{B}$	(0)	2
B	1	3



	I_0	I_1
$\bar{A}$	(0)	1
A	2	3
	$\bar{A}$	0



NAND gate using 2x1 MUX



① XNOR ⇒ $AB + \bar{A}\bar{B}$ ⇒ $A \odot B$.

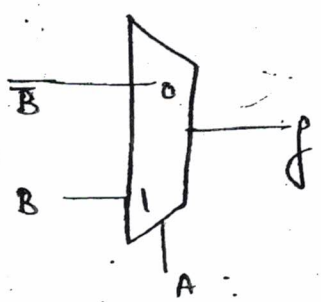
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

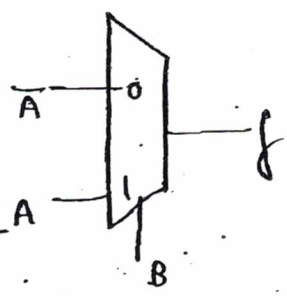
A as select line

	I_0	I_1
$\bar{B}$	(0)	2
B	1	(3)
	$\bar{B}$	B

B as select line

	I_0	I_1
$\bar{A}$	(0)	1
A	2	(3)
	$\bar{A}$	A





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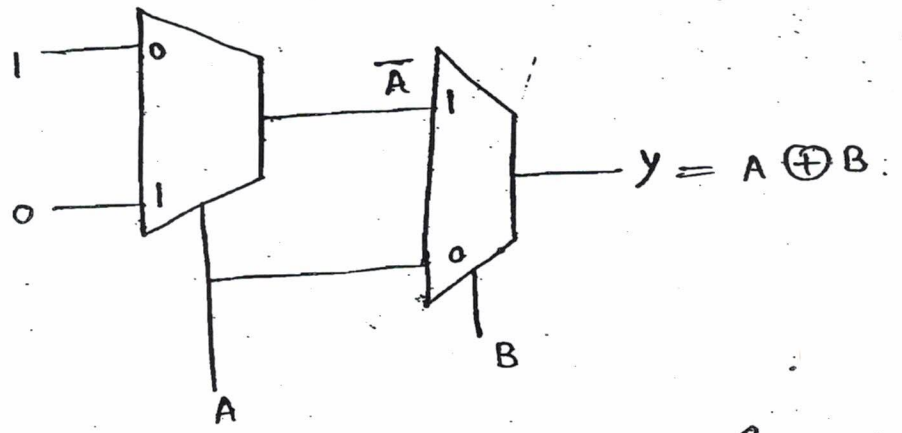
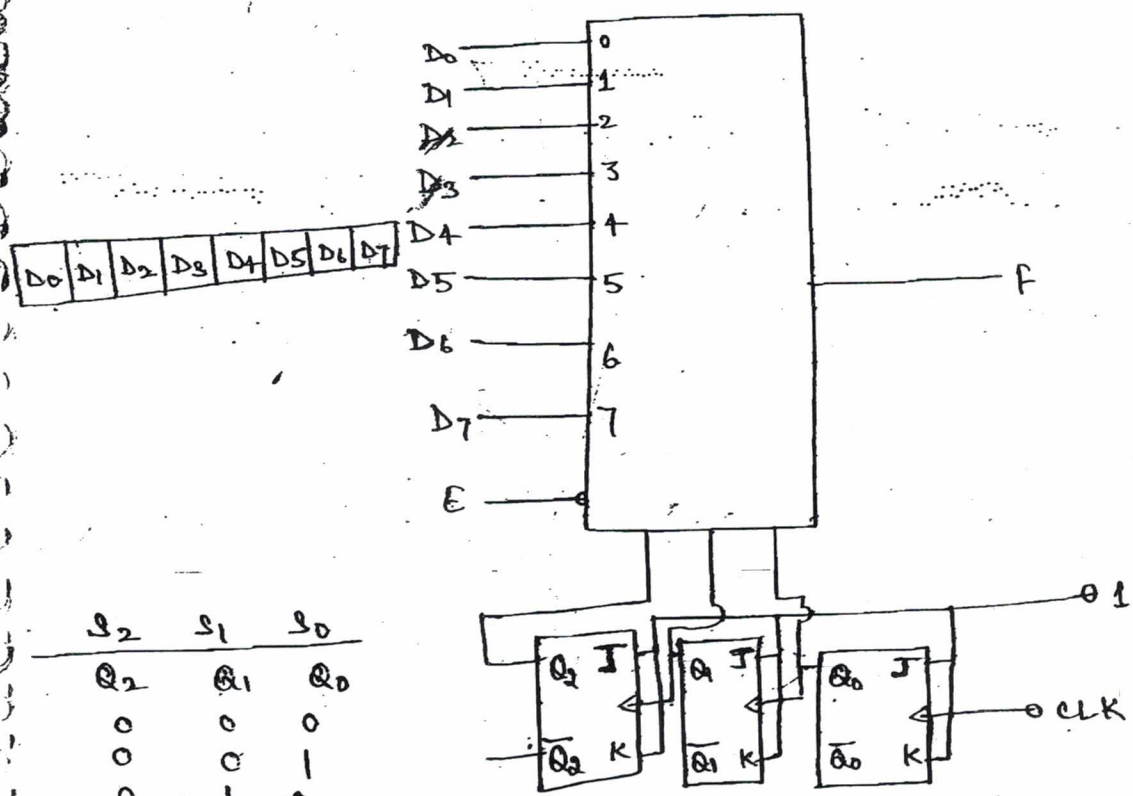
* XOR gate using 2, 2×1 mux



⇒ Because complemented i/p ($\bar{A}$ or $\bar{B}$) is not availab so use mux for complemented i/p.

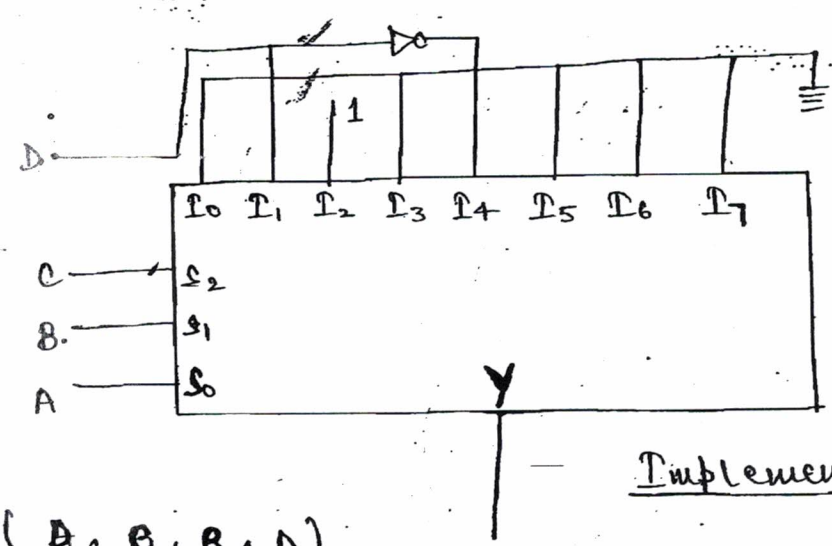
8 bit Parallel to Serial converter using MUX.



S_2	S_1	S_0
Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

E	S_2	S_1	S_0	f
H	X	X	X	0
L	0	0	0	D_0
L	0	0	1	D_1
L	0	1	0	D_2
L	0	1	1	D_3
L	1	0	0	D_4
L	1	0	1	D_5
L	1	1	0	D_6
L	1	1	1	D_7

Qus: Below figure shows the use of an 8×1 MUX to implement a certain 4 variable Boolean function from the given logic ckt arrangement, Derive boolean expression implemented by the given ckt



Implementation table

I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
0	1	(2)	3	(4)	5	6	7
8	(9)	(10)	11	12	13	14	15
0	D	1	0	$\bar{D}$	0	0	0

$f(D, C, B, A)$

$= \Sigma(2, 4, 9, 10)$. $\bar{D}$

$= \cancel{\bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} + A\bar{B}C\bar{D}}$ D

$\cancel{+ A\bar{B}C\bar{D}}$

$D\bar{C}B\bar{A} + \bar{D}C\bar{B}\bar{A} + D\bar{C}\bar{B}A + D\bar{C}B\bar{A}$

RS 115